REMARKS

The present amendment is in response to the Office Action dated December 3, 2002, where the Examiner has rejected claims 1, 3-7, 9-12, 14, 15 and 23. By the present amendment and response, the claims have been amended to overcome the Examiner's objections. Claim 3 has been cancelled. Accordingly, claims 1, 4-7, 9-12, 14, 15 and 23 are pending in the application. Reconsideration and allowance of pending claims 1, 4-7, 9-12, 14, 15 and 23 in view of the following remarks are respectfully requested.

A. Objection to Claims 1, 3-7, 9-12, 14-15 and 23 due to informalities

The Examiner has objected to claims 1, 7 and 23 and claims depending therefrom due to informalities. In particular, the Examiner has stated that the term "layerand" in claim 1 should be replaced with the term "layer and." To overcome the objection, Applicants have amended claim 1 to recite "layer and." The Examiner has further objected to the phrase "the insulator layer forming" in claim 1. To overcome the objection, Applicants have amended claim 1 to recite "the insulator layer is formed." Accordingly, Applicants respectfully submit that the objections to claim 1 have been traversed.

The Examiner has objected to the phrase "the tunnel oxide" in claim 7. To overcome the objection, Applicants have amended claim 7 to recite "the tunnel oxide layer." Accordingly, Applicants respectfully submit that the objection to claim 7 has been traversed.

The Examiner has objected to the phrase "the insulator layer of high quality oxide" in claim 23. To overcome the objection, Applicants have amended claim 23 to recite "the insulator layer of high quality oxide is formed on." Accordingly, Applicants respectfully submit that the objection to claim 23 has been traversed. Thus, Applicants respectfully submit that claims 1, 7 and 23 and claims depending therefrom are now in condition for allowance.

B. Rejection of Claims 1, 3-7, 9-12, 14-15 and 23 under 35 U.S.C. § 103(a)

The Examiner has rejected claims 1, 3, 5-7, 9, 11, 12 and 23 under 35 USC §103(a) as being unpatentable over **Wu** (USPN 6,033,956) ("**Wu '956**") or **Mitchell et al.** (USPN 4,713,142) ("**Mitchell '142**") in view of **Paterson et al.** (USPN 4,613,956) ("**Paterson '956**"). Although Applicants respectfully disagree with the Examiner's rejection, in order to expedite allowance of the present application, Applicants have amended independent claims 1, 7 and 23 in response to the Examiner's rejection. For the reasons discussed below, Applicants respectfully submit that amended independent claims 1, 7 and 23 and dependent claims 5-6, 9 and 11-12, are patentably distinguishable over **Wu '956**, **Mitchell '142**, **Paterson '956** or any combination thereof.

Pending claims 1, 7 and 23 are directed to methods of making a memory cell with a polished insulator layer. The present invention, as recited in amended independent claim 1, teaches, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the

tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer."

In contrast, **Wu '956**, **Mitchell '142** and **Paterson '956** do not, singly or in combination teach, disclose, or suggest a process that includes the above recited limitations specified by claim 1. In particular, **Wu '956** discloses a method to form contactless array for high density nonvolatile memories. **Wu '956** does not disclose, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer."

Mitchell '142 discloses a method for fabricating EPROM array. **Mitchell '142** does not disclose, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer."

Paterson '956 discloses a floating gate memory with improved dielectric. **Paterson '956** does not disclose, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking

from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer."

Applicants respectfully submit that there is no teaching or suggestion to combine **Wu '956**, **Mitchell '142** or **Paterson '956** to obtain a flash memory cell made by the method recited in amended independent claim 1. Thus, amended independent claim 1 and dependent claims 3 and 5-6 are patentably distinguishable over **Wu '956**, **Mitchell '142**, **Paterson '956** or any combination thereof.

The Examiner has rejected independent claim 7 for reasons similar to claim 1. Applicants have amended independent claim 7 to recite limitations similar to those recited in amended claim 1. In particular, claim 7 has been amended to recite, "[a] method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising: forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor; depositing a floating gate layer on the tunnel oxide layer to a first thickness; etching the floating gate layer, to provide a floating gate; depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to provide a planar surface

that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer." Thus, applicants respectfully submit that independent claim 7, having been amended to recite language similar that in claim 1, and its corresponding dependent claims should be allowed for at least the same reasons stated in conjunction with claim 1.

The Examiner has rejected independent claim 23 for reasons similar to claim 1. Applicants have amended independent claim 23 to recite limitations similar to those recited in amended claim 1. In particular, claim 23 has been amended to recite, "[a] method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer of high quality oxide is formed on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer." Thus, applicants respectfully submit that independent claim 23, having been amended to recite language

similar that in claim 1, should be allowed for at least the same reasons stated in conjunction with claim 1.

The Examiner has further rejected claims 4 and 10 under 35 USC §103(a) as being unpatentable over **Wu '956** or **Mitchell '142** taken with **Paterson '956** as applied to claims 1, 3, 5, 6, 7, 9, 11 and 23, and in further view of **Yamagishi et al.** (USPN 5,808,339) ("**Yamagishi '339**"). Applicants respectfully submit that the present invention, as defined by amended independent claims 1 and 7, from which claims 4 and 10 respectively depend from, is patentably distinguishable over **Wu '956**, **Mitchell '142**, **Paterson '956**, **Yamagishi '339** or any combination thereof. As discussed above, amended independent claims 1 and 7 are patentably distinguishable over **Wu '956**, **Mitchell '142** and **Paterson '956** and, as such, claim 4 depending from amended independent claim 1 and claim 10 depending from amended independent claim 7 are, *a fortiori*, also patentably distinguishable over **Wu '956**, **Mitchell '142** and **Paterson '956**.

Yamagishi '339 discloses a two-layered gate structure for a semiconductor device and method for producing the same. **Yamagishi '339** does not disclose, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of

high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer" or "[a] method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising: forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor; depositing a floating gate layer on the tunnel oxide layer to a first thickness; etching the floating gate layer, to provide a floating gate; depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer."

Applicants respectfully submit that there is no teaching or suggestion to combine **Wu '956**, **Mitchell '142**, **Paterson '956** or **Yamagishi '339** to obtain a flash memory cell made by the method recited in amended independent claims 1 and 7. As such, amended independent claims 1 and 7 and dependent claims 4 and 10 are patentably distinguishable over **Wu '956**, **Mitchell '142** and **Paterson '956** in combination with **Yamagishi '339**.

The Examiner has further rejected claims 14-15 under 35 USC §103(a) as being unpatentable over **Wu '956** or **Mitchell '142** taken with **Paterson '956** as applied to claims 1, 3, 5, 6, 7, 9, 11 and 23. Applicants respectfully submit that the present invention, as defined by amended independent claim 7, from which claims 14 and 15 depend from, is patentably distinguishable over **Wu '956, Mitchell '142, Paterson '956**. As discussed above, amended independent claim 7 is patentably distinguishable over **Wu '956, Mitchell '142** and **Paterson '956** and, as such, claims 14 and 15 depending from amended independent claim 7 are, *a fortiori*, also patentably distinguishable over **Wu '956, Mitchell '142**, and **Paterson '956**. Applicants respectfully submit that there is no teaching or suggestion to combine **Wu '956, Mitchell '142, Paterson '956** to obtain a flash memory cell made by the method recited in amended independent claim 7. As such, amended independent claim 7 and dependent claims 14 and 15 are patentably distinguishable over **Wu '956, Mitchell '142** and **Paterson '956**.

The Examiner has further rejected claims 1, 3-7, 9-12, 14-15 and 23 under 35 USC §103(a) as being unpatentable over by **Yamagishi '339** or **Chan et al.** (USPN 6,051,467) ("**Chan '467**") taken with **Sze et al.**, "ULSI Technology" ("**Sze**"). Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 7 and 23, from which claims 4-6, 9-12 and 14-15 depend from, is patentably distinguishable over **Yamagishi '339, Chan '467**, and **Sze**. As discussed above, amended independent claims 1, 7 and 23 are patentably distinguishable over **Yamagishi '339** and, as such, claims depending from amended independent claims 1, 7 and 23 are, *a*

fortiori, also patentably distinguishable over **Yamagishi '339**. Chan **'467** and **Sze** do not disclose, "[a] method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer" or "[a] method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising: forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor; depositing a floating gate layer on the tunnel oxide layer to a first thickness; etching the floating gate layer, to provide a floating gate; depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on

the planar surface directly over the exposed top surface of the floating gate and the insulator layer" or "[a] method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising: depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer of high quality oxide is formed on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process; polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer."

Applicants respectfully submit that there is no teaching or suggestion to combine **Yamagishi '339**, **Chan '467**, or **Sze** to obtain a flash memory cell made by the method recited in amended independent claims 1, 7 and 23. As such, amended independent claims 1, 7 and 23 and dependent claims 4-6, 9-12 and 14-15 are patentably distinguishable over **Yamagishi '339**, **Chan '467**, or **Sze**.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7 and 23, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 4-7, 9-12, 14, 15 and 23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 4-7, 9-12, 14, 15 and 23 pending in the present application is respectfully requested.

Respectfully Submitted,
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In the Claims:

Claim 1 has been amended as follows:

1. (Five Times Amended) A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide [layerand] layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer [forming] is formed around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing [a dielectric] an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Claim 3 has been cancelled.

Claims 7 and 23 have been amended as follows:

7. (Six Times Amended) A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

forming a first layer of a silicon dioxide on a floating gate of said floating gate transistor;

depositing a floating gate layer on the tunnel oxide layer to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing [a dielectric] an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

23. (Thrice Amended) A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer of high quality oxide is formed on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing [a dielectric] an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.